

WHAT IS CLAIMED IS:

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1. A process of manufacturing a semiconductor device comprising the steps of:

10 a) forming a stacked structure of a first III-V compound semiconductor layer containing In and having a composition different from InP and a second III-V compound semiconductor layer containing In, said second III-V compound semiconductor layer being formed over said first III-V compound semiconductor layer;

15 b) growing an InP layer at regions adjacent said stacked structure to form a stepped structure of InP; and

20 c) wet-etching said stepped structure and said second III-V compound semiconductor layer using an etchant containing hydrochloric acid and acetic acid to remove at least said second III-V compound semiconductor layer.

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2. The process as claimed in claim 1, wherein said etchant further contains at least one of water and hydrogen peroxide solution.

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35 3. The process as claimed in claim 1, wherein said etchant has a composition tailored such that, in said step c), an etching rate of said stepped structure and an etching rate of said second

III-V compound semiconductor layer are substantially equal.

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4. The process as claimed in claim 3, wherein said step a) is performed such that said second III-V compound semiconductor layer has a thickness that is substantially equal to a product of an etching rate of the InP layer using said etchant and an etching time of said step c).

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5. The process as claimed in claim 1, wherein said etchant has a composition tailored such that, in said step c), an etching rate of said stepped structure is lower than an etching rate of said second III-V compound semiconductor layer.

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6. The process as claimed in claim 1, further comprising the step of:

d) performing, after said step c), a further wet-etching process using a further etchant containing hydrochloric acid and acetic acid to obtain a planarized structure, said further etchant having a composition tailored such that an etching rate of said stepped structure is greater than an etching rate of said second III-V compound semiconductor layer.

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7. The process as claimed in claim 6,
wherein said further etchant further contains at
5 least one of water and hydrogen peroxide solution.

10 8. The process as claimed in claim 7,
wherein the relationship between an etching time T_1
in said step c) and an etching time T_2 in said step
d) is determined in accordance with an equation:

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$$(V_2 - V_1) \times T_1 = (V_3 - V_4) \times T_2,$$

20 where V_1 is an etching rate of the InP
layer in said step c);

V_2 is an etching rate of said second III-V
compound semiconductor layer in said step c);

V_3 is an etching rate of the InP layer in
said step d); and

25 V_4 is an etching rate of said second III-V
compound semiconductor layer in said step d).

30 9. The process as claimed in claim 1,
wherein said etchant has a composition tailored such
that, in said step c), an etching rate of said
stepped structure is greater than an etching rate of
35 said second III-V compound semiconductor layer.

10. The process as claimed in claim 9,
wherein said further etchant further contains at
5 least one of water and hydrogen peroxide solution.

10 11. The process as claimed in claim 9,
further comprising the step of:

d) performing, after said step c), a
further wet-etching process using a further etchant
containing hydrochloric acid and acetic acid to
15 obtain a planarized structure, said further etchant
having a composition tailored such that an etching
rate of said stepped structure is smaller than an
etching rate of said second III-V compound
semiconductor layer.

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12. The process as claimed in claim 11,
25 wherein the relationship between an etching time T_1
in said step c) and an etching time T_2 in said step
d) is determined in accordance with an equation:

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$$(V_1 - V_2) \times T_1 = (V_4 - V_3) \times T_2,$$

where V_1 is an etching rate of the InP
layer in said step c);

35 V_2 is an etching rate of said second III-V
compound semiconductor layer in said step c);

V_3 is an etching rate of the InP layer in

said step d); and

V_4 is an etching rate of said second III-V compound semiconductor layer in said step d).

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13. The process as claimed in claim 1, wherein said step b) further comprises the steps of:

10 forming a pattern covering said second III-V compound semiconductor layer on said stacked structure; and

growing an InP layer using said pattern as a growth mask,

15 wherein said step c) is performed with said stacked structure being protected by said pattern.

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14. The process as claimed in claim 13, further comprising the step of:

25 d) removing said pattern after said step c); and

e) performing a further wet-etching process using a further etchant containing hydrochloric acid and acetic acid to obtain a planarized structure, said further etchant having a composition tailored such that an etching rate of
30 said stepped structure is smaller than an etching rate of said second III-V compound semiconductor layer.

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15. The process as claimed in claim 14,
wherein said further etchant further contains at
least one of water and hydrogen peroxide solution.

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16. The process as claimed in claim 15,
wherein the relationship between an etching time T_1
in said step c) and an etching time T_2 in said step
e) is determined in accordance with an equation:

$$V_1 \times T_1 = (V_4 - V_3) \times T_2,$$

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where V_1 is an etching rate of the InP
layer in said step c);

V_3 is an etching rate of the InP layer in
said step e); and

V_4 is an etching rate of said second III-V
compound semiconductor layer in said step e).

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17. The process as claimed in claim 1,
wherein, after said step c), said stepped structure
is provided with a planarized surface formed of a
(100), (011) or (0-1-1) surface.

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18. The process as claimed in claim 17,
wherein said planarized surface is substantially
flush with the surface of said first III-V compound

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semiconductor layer.

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19. The process as claimed in claim 1, wherein, after said step c), said stepped structure is provided with a planarized surface near a (100), (011) or (0-1-1) surface.

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20. The process as claimed in claim 1, wherein said second III-V compound semiconductor layer has a composition chosen from a group consisting of InP, InGaAs, InAs, InGaP, InGaAsP and GaInNAs.

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21. The process as claimed in claim 1, wherein said first III-V compound semiconductor layer has a composition chosen from a group consisting of InGaAs and InGaAsP.

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